REPLACEMENT

PAGES

WITH MARKINGS

TO SHOW CHANGES

10. These and other multipliers may be used with various embodiments of the present invention.

In operation with the sampling frequency signal 114 operating for the duration of the current example at 1000 Hz, a first counter register 260 will count low to high transitions on the oscillator 252 output (out) 256 clocking signal 254, which is operating at 1 MHz. A second counter register 272 will count low to high transitions on a scaled oscillator signal 266 received from an output (out) 268 of a frequency divider 264, which is operating at 100 kHz until the second counter register 272 is reset at 288 by a low to high transition of the sampling frequency signal 114. In the present example, a compare register 280 will have a value of 100 at its input terminal (in1) 278. That value of 100 is equal to the number of low to high transitions received at a clock terminal (clk) 270 of the second counter register 272 between individual low to high transitions of the sampling frequency signal 114, i.e., 100 kHz divided by 1000 Hz, or a count of 100. The compare register 280 will furthermore transition its output from low to high each time the count signal 284 received from the output (out) 282 of the first counter register 260 at its input (in2) 286 reaches a value equal to the value of a signal 276 received from an output (out) 274 of the second counter register 272 at its other input (in1) 278. Thus, the compare register output (out) 292 will transition each time the count at input (in2) 286 reaches 100 in the present example. Because the frequency of the signal 254 provided to the clock terminal (clk) 258 of the first counter register 260 is ten times greater than the frequency of the signal 266 provided to the clock terminal (clk) 270 of the second counter register 272, a compare register output (out) 292 will transition ten times for each transition of the sampling frequency signal 114 received at a load terminal 290. When the compare register output (out) 292 transitions, the output signal 294 of the compare register 280 will reset the first counter register 260 at 296 and trigger a toggle register 300 at 298. The toggle register 300 then provides a filter control signal 108 at output (out) 302 that operates at a frequency ten times greater than that of the sampling frequency signal 114. It will be recognized that the filter control signal 108 provided to the clock-tunable filter 104 may be set to operate at a frequency that

may be any desired multiple of the sampling frequency signal 114 by selecting a frequency divider 264 that divides the oscillator clocking signal 254 received at input (in) 262 by the desired multiple.

The embodiments of the invention lend several important features to the design of a filter for a signal having a changing sampling rate: (i) the filter frequency may always be set in direct proportion to the sampling frequency; (ii) the signal delay may always be set to a fixed number of samples, and can be arranged to be a single sample point delay if the filter frequency is set at an appropriate value; and (iii) the system is capable of following any sampling rate set by the system without external intervention.

The present invention produces a very adaptable anti-aliasing filter system for high-speed data acquisition where there is little or no communication with the host computer and yet the filter is always set to the most suitable condition. The application of this idea may be universally applied to any data acquisition application in which an anti-aliasing hardware filter is required or desired to ensure accurate logging of data and subsequent software filtering.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof. In particular, it should be noted that the present invention provides a filter having a frequency that will adjust to any sampling signal including signal operating at a constant sampling rate and a signal operating at a variable sampling rate. Thus, the present invention also beneficially provides a filter that may be used in a constant sampling application without requiring manual set-up by an operator. Thus, it is intended that the present invention cover modifications and variations of this invention provided that they come within the scope of the appended claims and their equivalents.

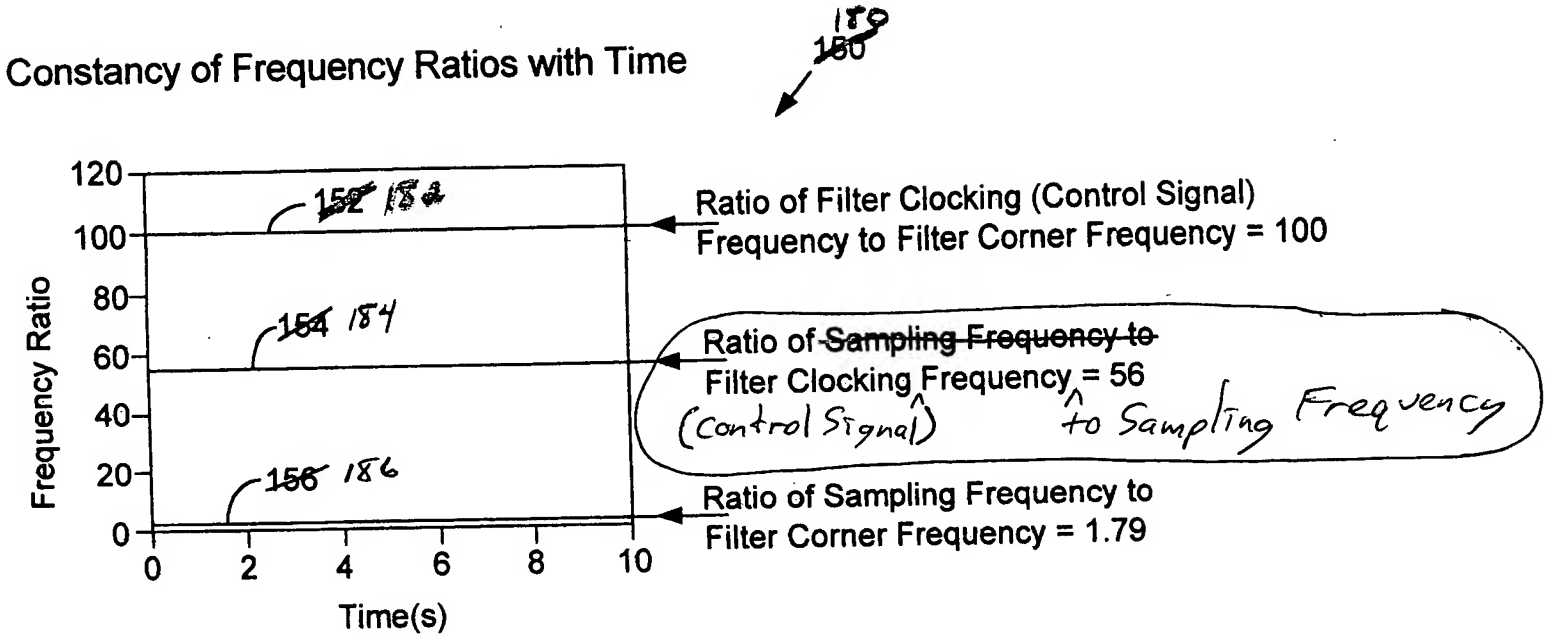

Figure 3/7